BasicBoard

FPGA Development and Evaluation Board

User Manual

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http://www.coreworks.pt

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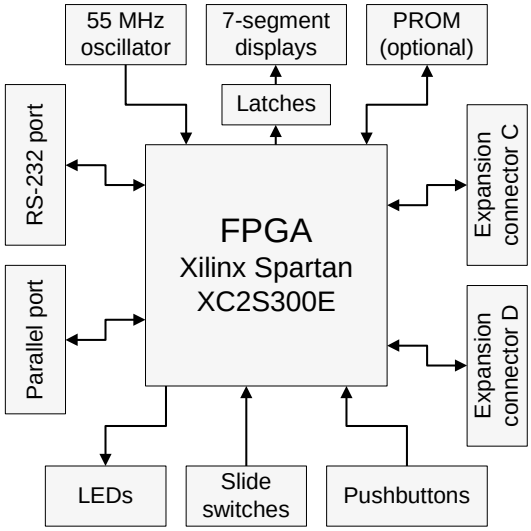
Block Diagram of the BasicBoard



FEATURES

- **Features a Xilinx Spartan-IIE FPGA XC2S300E with a capacity of 300,000 equivalent system gates.**
- **Resources for basic lab work: five pushbuttons, eight LEDs, four 7-segment displays, and eight slide switches.**
- **Includes a 55 MHz oscillator useful as a system clock.**
- **Parallel Port for FPGA configuration and communication purposes.**
- **RS-232 interface for serial communication.**
- **Includes two 40-pin expansion connectors, with 74 general-purpose I/Os and 3 FPGA Global Clock Inputs.**
- **Designed to mate with other Coreworks peripheral by means of the expansion connectors.**
- **Typical applications: basic lab teaching, specific applications using dedicated boards plugged to the expansion connectors (audio, video, etc).**

DESCRIPTION

The BasicBoard is an FPGA development and evaluation board suitable for implementation of a wide range of application circuits. The board features a Xilinx Spartan-IIE FPGA (XC2S300E) which has a capacity for implementing circuits with up to 300K system gates of complexity.

A simplified layout of the BasicBoard is shown in Figure 1.

The BasicBoard provides an assortment of the most frequently used interfaces for basic laboratory work. These interfaces include eight slide switches, five pushbuttons, eight LEDs and four 7-segment displays. There are also two independent expansion connectors with a total of 74 general purpose I/O pins connected directly to the FPGA, 3 Global Clock inputs (GCK) and 3 power pins (3.3 VDC, Ground and Voltage Unregulated).

For basic communication with a PC or other equipment, the board includes an RS-232 port and a parallel port.

The parallel port is used to send the configuration file to the FPGA. Alternatively, the configuration can be stored in a PROM and loaded at power-up. The PROM is an optional component and a socket is provided for it.

The BasicBoard is designed to mate with other Coreworks boards by means of the expansion connectors C and D.

This document describes the main blocks available in the BasicBoard. All input/output interfaces are described, in particular, as well as the mapping between the FPGA pins and each I/O interface. The FPGA configuration options are also described.

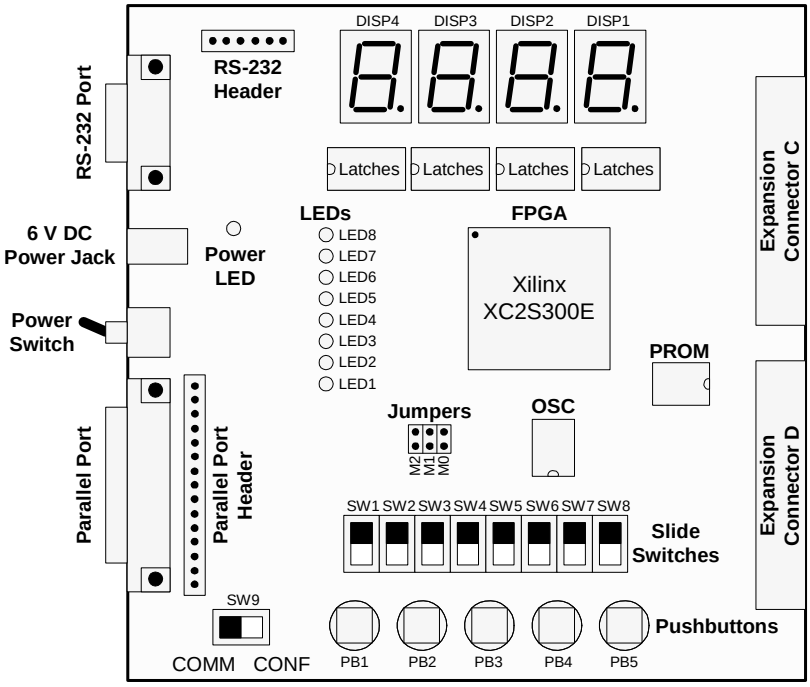


Figure 1: Simplified layout of the BasicBoard.

POWER SUPPLY

The BasicBoard uses a 6V DC power supply. The power supply should have a 2.1 mm female, center-positive plug and be capable of delivering at least 500 mA.

The board can be switch on and off using the power switch next to the power jack. The board is properly powered when the Power LED is turned on.

JUMPER SETTINGS

The jumpers select the FPGA configuration mode. Please see the next section ("FPGA Configuration") for further details.

By default the jumpers M0, M1 and M2 are not placed.

FPGA CONFIGURATION

The FPGA configuration can be loaded from a PC parallel port or from a PROM (not included in the kit).

Typically the FPGA configuration is loaded from a PC. In this situation, the parallel port should be used. The signals required by the JTAG programming mode pass throughout this port. To support the JTAG mode, additional circuitry is included in the BasicBoard.

In order to prevent a communication failure between the PC and the FGPA, the power supply must be turned on before attaching the parallel cable.

To load the configuration from a host computer, follow these steps:

1. apply power to the board,
2. attach the parallel cable (included in the kit) between the PC and the parallel port connector of the BasicBoard,
3. set the slide switch SW9 to the CONF position,
4. remove all jumpers (M0, M1 and M2),
5. run the appropriate configuration software in the PC (e.g., IMPACT from Xilinx).

To configure the FPGA from a PROM, follow these steps:

1. place the programmed PROM into the 8-pin socket labeled PROM,
2. set the slide switch SW9 to the COMM position,
3. add all jumpers (M0, M1 and M2),
4. power-on the board.

BASICBOARD COMPONENTS

The BasicBoard provides the following resources:

- one 55 MHz crystal oscillator
- eight leds;
- four 7-segment displays;
- eight slide switches;
- five pushbuttons;
- one RS-232 port;
- one Parallel port;
- two 40-pin expansion connectors.

These resources are shown in the simplified layout of the BasicBoard (Figure 1), and are described in the following sections.

OSCILLATOR

The BasicBoard is shipped with a 55 MHz oscillator, whose output is connected to the FPGA GCK0 input (pin 80). The oscillator module is assembled in an 8-pin socket labeled OSC. When a different frequency is required, this oscillator can be replaced by any compatible device.

LEDS

The BasicBoard provides eight individual LEDs. All of these LEDs are active-high. Table 1 shows the FPGA pins connected to the LEDs.

LED	FPGA pin
LED1	40
LED2	36
LED3	35
LED4	34
LED5	33
LED6	31
LED7	30
LED8	29

Table 1: FPGA pins for the LEDs.

SEVEN-SEGMENT DISPLAYS

The BasicBoard provides four seven-segment displays. Each seven-segment display is driven by external D-type latches. The latches are grouped in arrays of 8 latches (one array for each seven-segment display). Each array is addressed by an enable signal provided by the FPGA (see Table 2). The latch is writable when the enable signal is pulled high.

Display	FPGA pin
DISP1	176
DISP2	178
DISP3	179
DISP4	180

Table 2: FPGA pins for the latch enable signal of each display.

Each segment in each enabled display is controlled by an FPGA output. The segment turns on, when the FPGA output is pulled to ground (active-low signal). Table 3 shows the FPGA pins for driving the latches of each segment.

Segment	FPGA pin
A	194
B	193
C	192
D	191
E	189
F	188
G	187
Point	181

Table 3: FPGA pins for the segment drivers (latches).

SLIDE SWITCHES

The BasicBoard contains an array of eight slide switches. When closed or ON, each slide switch pulls the FPGA pin to ground. When the slide switch is open or OFF, the pin is pulled high. Table 4 shows the mapping between the FPGA pins and each slide switch.

Slide switch	FPGA pin
SW1	49
SW2	55
SW3	56
SW4	57
SW5	58
SW6	59
SW7	60
SW8	61

Table 4: FPGA pins for the slide switches.

PUSHBUTTONS

The BasicBoard has five pushbuttons. When pressed, each pushbutton pulls the FPGA pin to VDD. Otherwise, the pin is pulled to ground through a resistor. The connections between the FPGA and the pushbuttons are presented in Table 5.

Pushbutton	FPGA pin
PB1	62
PB2	63
PB3	64
PB4	68
PB5	69

Table 5: FPGA pins for the pushbuttons.

RS-232 PORT

The BasicBoard has a 9-pin RS-232 port that provides an interface to transmit and receive serial data streams (TXD and RXD, respectively), as well as the flow control signals (RTS, CTS and DSR). The pin functions on the BasicBoard RS-232 port are identical to those found on a PC serial port. When the BasicBoard and the PC are to communicate, a DTE-to-DCE cable (straight-thru cable) should be used. Table 6 shows the mapping between the FPGA pins and the RS-232 interface. The RS-232 pinout is shown in Figure 2.

RS-232 signal	RS-232 pin	FPGA pin	Direction	RS-232 Function
RXD	3	202	I	Receive Data
TXD	2	201	O	Transmit Data
DSR	6	200	O	Data Set Ready
RTS	7	198	I	Request to Send
CTS	8	199	O	Clear to Send

Table 6: FPGA pins for the RS-232 port.

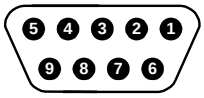


Figure 2: RS-232 connector (front view).

PARALLEL PORT

The BasicBoard contains a parallel port connector (25-pins female connector). This interface establishes a communication channel between a computer and the FPGA.

The BasicBoard supports both SPP (Simple Parallel Port) and EPP (Enhanced Parallel Port – IEEE 1284) protocols. The EPP protocol is highly recommended because provides a bidirectional data channel and a much higher data transfer rate (see Table 7).

NOTE: The parallel port must be configured to the selected protocol (SPP or EPP). In a PC, the parallel port protocol is changed in the BIOS setup. To enter the BIOS setup, the appropriate key (F2, DEL, etc.) must be pressed while the system is starting up.

Port Mode	Maximum Transfer Rate (MB/s)	Direction
SPP	0.15	Unidirectional (PC ⇒ BasicBoard)
EPP	2	Bidirectional

Table 7: Comparison between SPP and EPP modes.

The FPGA configuration can be loaded using the parallel port interface. The slide switch SW9 toggles between the configuration mode (CONF position) and the normal communication (COMM position).

Table 8 shows the mapping between the FPGA pins and the parallel port interface. The parallel port pinout is shown in Figure 3.

Signal name	Connector pin	FPGA pin	Direction	EPP Function
PWE	1	206	O	Write Enable
PD0	2	15	I/O	Address/Data 1
PD1	3	11	I/O	Address/Data 2
PD2	4	10	I/O	Address/Data 3
PD3	5	9	I/O	Address/Data 4
PD4	6	8	I/O	Address/Data 5
PD5	7	7	I/O	Address/Data 6
PD6	8	6	I/O	Address/Data 7
PD7	9	5	I/O	Address/Data 8
PINT	10	4	I	Interrupt
PWT	11	3	I	Wait
–	12	–	–	not connected
–	13	–	–	not connected
PDS	14	205	O	Data Strobe
–	15	–	–	not connected
PRS	16	203	O	Reset
PAS	17	204	O	Address Strobe
–	18-25	–	–	Ground

Table 8: FPGA pins for the parallel port (EPP Mode).

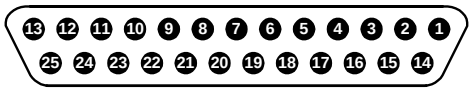


Figure 3: Parallel port (front view).

EXPANSION CONNECTORS

Expansion boards with specialized circuitry can be connected to the BasicBoard through expansion connectors C and D. The connector pins have a pitch (spacing) of 100 mils (or 2.54 mm). The ground (GND) is available on pin 1 of connector C (C01), the VDD (3.3 V) is routed to pin C03, and pin C02 provides a Voltage Unregulated (VU) signal (direct connection to the voltage provided by the 6 V DC power jack). All other pins in connectors C and D are routed directly to the FPGA.

Among those pins, three of them are connected to dedicated FPGA clock pins. These inputs are available in pins C05, C19 and C29 (connector C).

Table 9 shows the mapping between the FPGA pins and the expansion connectors C and D.

Most of the pins available in the expansion connectors can be used as general-purpose pins (see Table 9). However, some pins can be used to access specific resources in the FPGA (Digital Looked Loops (DLLs), Threshold Reference Voltages, etc.). For further information on the Spartan XC2S300E pinout, please see the datasheets available at the Xilinx website (www.xilinx.com).

Connector C				Connector D			
Pin	**Name**	**FPGA pin**	**Direction**	**Pin**	**Name**	**FPGA pin**	**Direction**
C01	**GND**	**–**	**O**	D01		45	I/O
C02	**VU**	**–**	**O**	D02		44	I/O
C03	**VDD 3.3 V**	**–**	**O**	D03		46	I/O
C04		16	I/O	D04		125	I/O
C05	**GCK3 Input**	**185**	**I**	D05		122	I/O
C06		17	I/O	D06		123	I/O
C07		175	I/O	D07		47	I/O
C08		174	I/O	D08		121	I/O
C09		173	I/O	D09		115	I/O
C10		169	I/O	D10		23	I/O
C11		168	I/O	D11		113	I/O
C12		167	I/O	D12		114	I/O
C13		166	I/O	D13		111	I/O
C14		165	I/O	D14		112	I/O
C15		164	I/O	D15		109	I/O
C16		163	I/O	D16		110	I/O
C17		162	I/O	D17		102	I/O
C18		20	I/O	D18		48	I/O
C19	**GCK2 Input**	**182**	**I**	D19		100	I/O
C20		154	I/O	D20		101	I/O
C21		152	I/O	D21		98	I/O
C22		151	I/O	D22		99	I/O
C23		150	I/O	D23		96	I/O
C24		149	I/O	D24		97	I/O
C25		148	I/O	D25		94	I/O
C26		147	I/O	D26		95	I/O
C27		146	I/O	D27		89	I/O
C28		21	I/O	D28		93	I/O
C29	**GCK1 Input**	**77**	**I**	D29		87	I/O
C30		140	I/O	D30		88	I/O
C31		139	I/O	D31		84	I/O
C32		138	I/O	D32		86	I/O
C33		136	I/O	D33		82	I/O
C34		22	I/O	D34		83	I/O
C35		134	I/O	D35		75	I/O
C36		133	I/O	D36		81	I/O
C37		132	I/O	D37		73	I/O
C38		129	I/O	D38		74	I/O
C39		127	I/O	D39		70	I/O
C40		43	I/O	D40		71	I/O

Table 9: FPGA pins for the expansion connectors C and D.