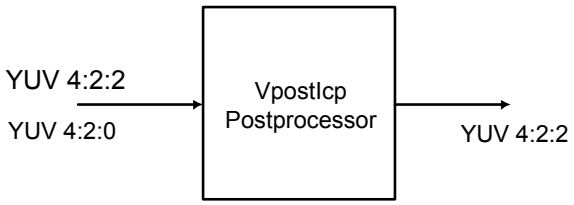
Philips Semiconductors

VpostIcp is a TSSA compliant software library that performs video postprocessing functionality in a streaming video, but also in a still picture use case.

VpostIcp



Description

The video postprocessor performs video postprocessing functionality for streaming and still picture use cases. For scaling, YUV 4:2:0 to YUV 4:2:2 conversion, deinterlacing and flicker filtering, the ICP coprocessor is being used. Rotation, intended for the still use cases, is performed in software and will not work in real time for streaming video. Flicker filtering is also in software available.

The video postprocessor is designed to operate with upstream decoders like MPEG-2, MPEG-4, JPEG, BMP and the usual video renderer as downstream component. The targetted display type is a TV set, possibly with progressive display capabilities.

Therefore, the video postprocessor only operates on the YUV color space and does not support the capability of the ICP coprocessor to output a RGB image through the PCI bus to a graphics card. This is also the most important difference with VtransIcp.

The input buffering feature enables that the control application can e.g. rotate a still picture differently without having to re-read/decode the still picture.

Applications

- Multimedia playback applications

Documentation

A detailed document describing the API and the internal behaviour of the component is available.

Features:

- Horizontal up- and down scaling.
- Vertical up- and down scaling Vertical scaling can be done either frame or field based
- YUV 4:2:0 to YUV 4:2:2 conversion
- Deinterlacing
- Flicker filtering
- Input windowing
- Input buffering
- Background management
- Rotation of the picture by 90, 180 or 270°

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VpostIcp

Technical Information

Memory Usage

Static Memory	appr. 64 KBytes
Dynamic Memory	appr. 1110 Kbytes

The dynamic memory is mainly required for two intermediate buffers that can hold a full-D1 PAL, rotated YUV 4:2:2 picture. Applications that only operate on smaller resolutions or do not apply rotation can adapt the size of the intermediate buffers.

Additional memory is required for buffering of input and output data. This amount is application-dependent.

Processor Load (MIPS)

For a component like VpostIcp, not only the DSPCPU task load is of interest, but also the load of the ISR, the required memory bandwidth and the ICP coprocessor load. We will illustrate this by showing the results of typical, best case and/or worst case scenarios using both MPEG-4 and MPEG-2 video playback.

Measurements are done using a IREF board equipped with a PNX130x running at 178.75MHz with a ratio of 4:5 (SD-RAM clocked at 143 MHz).

	VpostIcp task load (MIPS)	ICP ISR load (MIPS)	ICP load (%)
MPEG-2, 704*576@25Hz. YUV 4:2:0 to YUV 4:2:2 conversion	1.6	0.2	25
MPEG-2, 704*576@25Hz Scale to 720*480 YUV 4:2:0 to YUV 4:2:2 conversion Deinterlace	1.4	1.1	87
MPEG-4, 348*240@25Hz YUV 4:2:0 to YUV 4:2:2 conversion	1.3	0.2	5
MPEG-4, 348*240@25Hz Scale to 720*576 YUV 4:2:0 to YUV 4:2:2 conversion	1.3	0.4	40

Other Information

Supported Processors	TM-1100, TM-1300
Version	1.4
Built with Compiler Version	V5.7.1 of tcs2.2-dvp0003WinNT

Related TriMedia TSSA Software Components

VdecBmp, VdecJpeg, VdecGif, VdecMpeg, VdecMpeg4, VrendVo, VtransIcp

Example Programs

- exolMpeg4, which is used for upscaling. and YUV 4:2:0 to 4:2:2 conversion.

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