THIS APPLICATION CAN BE DONE USING:

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Costas Loop Implementation with Hypersignal® Block Diagram/RIDE™

Overview

Hypersignal Block Diagram/RIDE is a comprehensive visual design, simulation and real time tool for DSP applications such as communications, radar, sonar, speech processing, and image processing. The following example of design and simulation techniques using Hypersignal Block Diagram/RIDE features a Costas loop which is popularly used in the carrier recovery of demodulators. Carrier recovery (sometimes referred to as phase referencing) is the operation of extracting a phase coherent reference carrier from an observed noisy received carrier. When the received carrier is phase modulated such as BPSK (Binary Phase Shift Keying) or QPSK (Quadrature Phase Shift Keying), there is no direct carrier component to be tracked, and carrier recovery can not be obtained via a standard phase locked loop. Instead a modified system must be used, which must first use a non-linearity to eliminate (wipe-off) the modulation while creating a carrier component having a phase variation proportional to that of the received carrier. Subsequent tracking of this residual carrier component then generates the desired carrier reference. The Costas, or quadrature, loop is a common method for achieving this carrier recovery.

Product Specific Information

The Costas Loop Implementation described in this application note was created with Hypersignal RIDE Enterprise Edition (HSWN8200). The primary advantage of this package is that all modes of operation are supported: simulation, direct operation on DSP, object code generation, and ANSI C source code generation. Any Hypersignal Block Diagram/RIDE or OORVL Design Studio Edition can reproduce the results generated for this report.

Detailed Description

The classical Costas loop that is suitable for BPSK/QPSK demodulation is shown in the Figure 1. The system involves two parallel tracking loops operating simultaneously from the same VCO (Voltage-Controlled Oscillator) or NCO (Numerically-Controlled Oscillator). The first loop, called the in-phase loop (or I arm), uses the VCO as in a PLL (Phase Locked Loop), and the second, called the quadrature loop (or Q arm) uses a 90 degree shifted VCO. The I and Q mixer outputs are filtered by single pole Butterworth low pass filters. The I and Q arm filter outputs are multiplied together and the product is scaled and filtered to produce the loop error used to control the VCO. The loop error should settle to a value when the loop is locked. A negative loop error decreases the VCO increment resulting in a lower VCO frequency, and similarly, a positive loop error increases the VCO increment resulting in a higher VCO frequency. The low pass filters in each arm must be wide enough to pass the data modulation without distortion.

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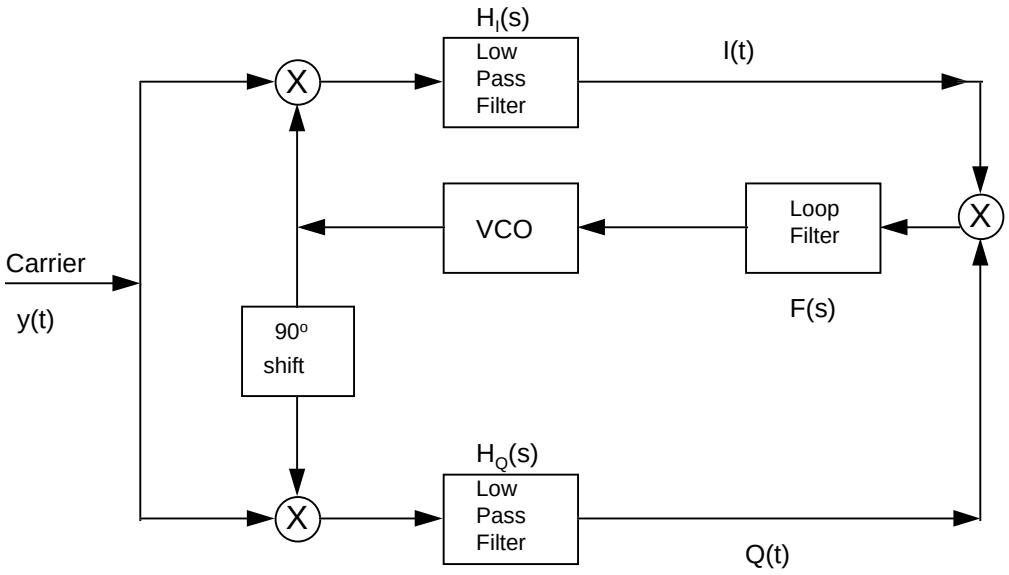

Figure 1. Costas Loop Block Diagram

The input to the Costas loop is the waveform written as

$$y(t) = m(t)*\sin(\omega_c t + \psi(t)) + n(t)$$

where m(t) is the BPSK modulation and n(t) is a white bandpass noise. The in-phase mixer generates

$$I(t) = m(t)*\cos\psi_e + n_{mc}(t)$$

while the quadrature mixer generates

$$Q(t) = m(t)*\sin\psi_e + n_{ms}(t)$$

where the mixer noise $n_{mc}(t)$ and $n_{ms}(t)$ are low pass demodulated noise processes in the carrier noise n(t). The output of the multiplier is then

$$I(t)Q(t) = m^2(t)\sin(2\psi_e)/2 + n_{sq}(t)$$

where $n_{sq}(t)$ represents all the signal and noise cross-products. The multiplier of the Costas loop can be thought of as allowing the bit polarity of the in-phase loop to correct the phase error orientation of the tracking loop, thereby removing the modulation. When the phase error $\psi_e(t)$ is small, the Costas loop has the equivalent linear model in Figure 2.

Implementation

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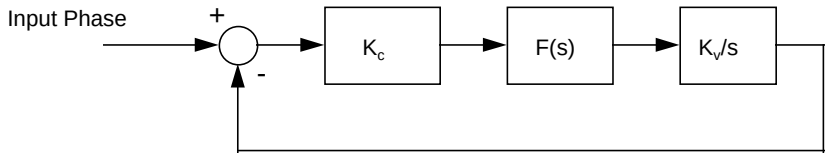

Figure 2. BPSK Costas Equivalent Loop Model

In above figure, K_c is the closed loop gain, which can be expressed as

$$K_c = (m(t)/2)^2 H_I(0) H_Q(0) g_c$$

where g_c is defined as follows

$$g_c = 4\omega_c / (K_v m^2(t) H_I(0) H_Q(0))$$

and where ω_c is the cross-over frequency, K_v is the gain of VCO, and F(s) is the transfer function of the loop filter, which is expressed in the following equation

$$F(s) = (sT + 1) / sT$$

where T is the sampling interval. The transfer function of the VCO is K_v/s .

Power Detect and Lock Detect

An interesting property of Costas loops is that the loop generates signals that can be used for other auxiliary purpose as well. This can be seen by reexamining the in-phase mixed signal and noting the following:

$$I(t)|_{\psi e = 0} = Am(t)$$

This shows that when the loop is locked, the in-phase arm produces an output proportional to the input data. Hence the data can be demodulated directly within the Costas loop after phase lock occurs.

$$I^2(t) - Q^2(t) = A^2 m^2(t) \cos(2\psi_e)$$

Squaring, low pass filtering, and subtracting the arm voltages produces an output that indicates phase lock [$\cos(2\psi_e)$->1 as ψ_e->0] and can therefore serve as a lock detector. When ψ_e = 0, this generates an output proportional to the average signal power, which can also be used for automatic gain control.

$$I^2(t) + Q^2(t) = A^2 m^2(t) + n^2_{ms} + n^2_{mc}$$
$$= \text{Total power of } y(t)$$

This produces a measurement of the total RF input power, and therefore can be used for RF power control. The modified Costas loop is shown in Figure 3.

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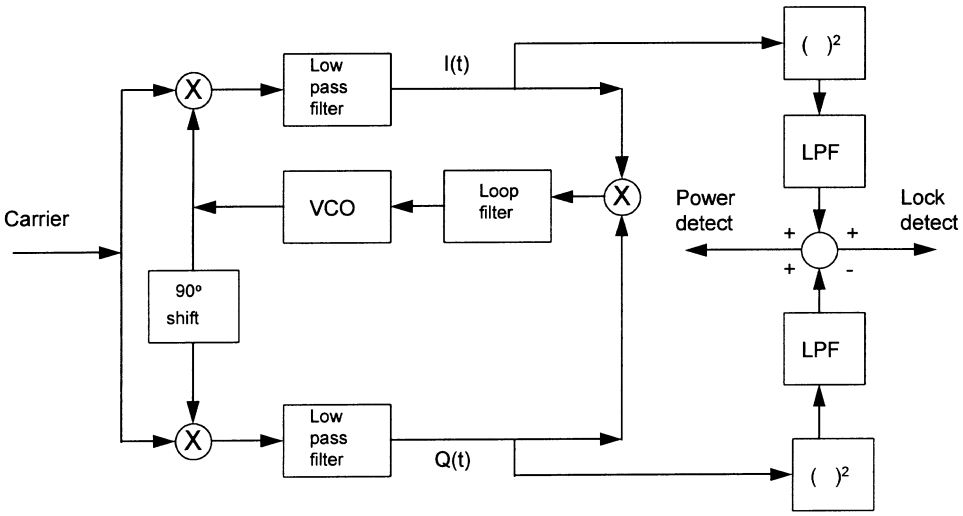

Figure 3. The Modified Costas Loop with Power and Lock Detects

Digital Implementation

Due to continuing advances in high-speed digital technology, digital implementations of the Costas loop are becoming increasingly attractive. Advantages of digital implementations include their relative insensitivity to temperature variations and aging. More importantly, however, is the unique advantage that the loop design parameters, such as loop gain and loop filter time constant, can be programmable.

The low pass filters, $H_I(s)$ and $H_Q(s)$ each have the same format consisting of a single pole, this can be expressed as

$$H(s) = H(0)/(1+s/\omega_a)$$

where ω_a is the cut-off frequency, H(0) is equal to $(\tan(\omega_a T/2)+1)/\tan(\omega_a T/2)$. The signal flow graph for this first order system is shown in Figure 4.

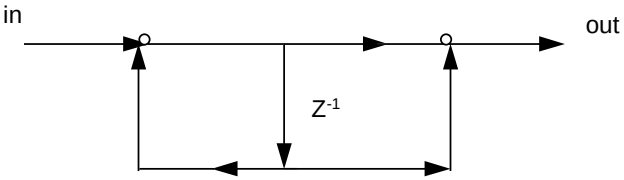

Figure 4. First Order Low Pass Filter Model

In the above figure, b is calculated as follows

$$b = (1 - \tan(\omega_a T/2)/(1 + \tan(\omega_a T/2)$$

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The signal flow graph of the first order loop filter is shown in Figure 5,

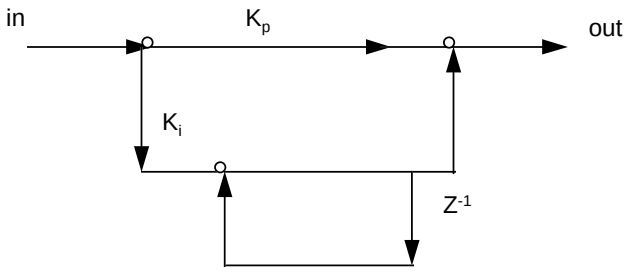

Figure 5. First order Loop Filter Model

In the above figure, K_p is the proportional gain which equals g_c, and K_i is the integral gain, which is can be expressed as

$$K_i = g_c T \omega_Z$$

where ω_Z is the zero frequency of the loop filter.

Traditional Design Method

The design of the Costas algorithm includes compromises between algorithm complexity and performance objectives. Typically the designer sketches out a signal flow graph of the algorithm using "Black Boxes" to represent signal processing operations. The computational requirements can be estimated from the signal flow graph by counting the number of multiplies, multiply-accumulate, and additions. A block diagram of the system can then be drawn out.

Once the algorithm has been worked out on paper, a simulation program may be written to verify that the concept is correct. The simulation has quite often been written in the past using high level language such as C and FORTRAN. Unless the designer is also highly skilled in programming, the simulation software can require a long time to write and debug. This is because errors in the algorithm can be mistaken for programming errors or vice versa. Analyzing algorithmic trade-offs is more difficult because the software must be modified and debugged while changing or modifying subsystems. Viewing and analyzing the results of a simulation typically requires the use of a different software package or writing and debugging special display programs. And finally, testing can also prove to be very time consuming.

Designing with Hypersignal Block Diagram/RIDE

In order to reduce design time and to make the design portable, it would be advantageous to use a tool that would allow the designer not only to document algorithms in a signal flow graph format, but also to automatically generate a simulation from that documentation. The tasks of signal generation, viewing, manipulation, and verification also need to be addressed. These are precisely the needs that are fulfilled by the Hypersignal line of visual DSP software development tools.

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Hypersignal Block Diagram/RIDE offers many advantages over other design methods. Designs are visually entered into the Block Diagram as signal flow diagrams. It is very easy to understand the function and operation of an algorithm when it is shown in this form, and this especially valuable when the designer is not personally implementing the algorithm on the target hardware.

Our example is implemented with the following parameters:

Sampling frequency:	106666.66 Hz
In-phase low pass filter cut-off frequency :	12000 Hz
Quadrature low pass filter cut-off frequency:	24000 Hz
Lock low pass filter cutoff frequency:	500 Hz
Loop filter cross-over frequency(Acq):	1000 Hz
Loop filter zero frequency(Acq):	500 Hz
Loop filter cross-over frequency(Track):	125 Hz
Loop filter zero frequency(Track):	25 Hz
Lock threshold value:	9950
Carrier frequency:	27000 Hz
NCO higher frequency limit:	27666.66 Hz
NCO lower frequency limit:	25666.66 Hz
NCO maximum input value:	2000
NCO minimum input value:	-2000

Based on the algorithm described in above section, we calculated the following coefficients:

The in-phase (I) arm filter coefficient is:	$b_I = 0.461006$
The quadrature (Q) arm filter coefficient is:	$b_Q = 0.0787017$
The lock detector low pass filter cofficient is:	$b = 0.970900$,
The loop filter coefficients for acquisition are:	$K_i = 1.123229$, $K_p = 38.136880$,
The loop filter coefficients for tracking are:	$K_i = 0.140402$, $K_p = 4.767110$,
The NCO gain is:	$K_v = 0.500000$.

Figure 6 presents a worksheet of the Costas loop, which implements the diagram in Figure 3.

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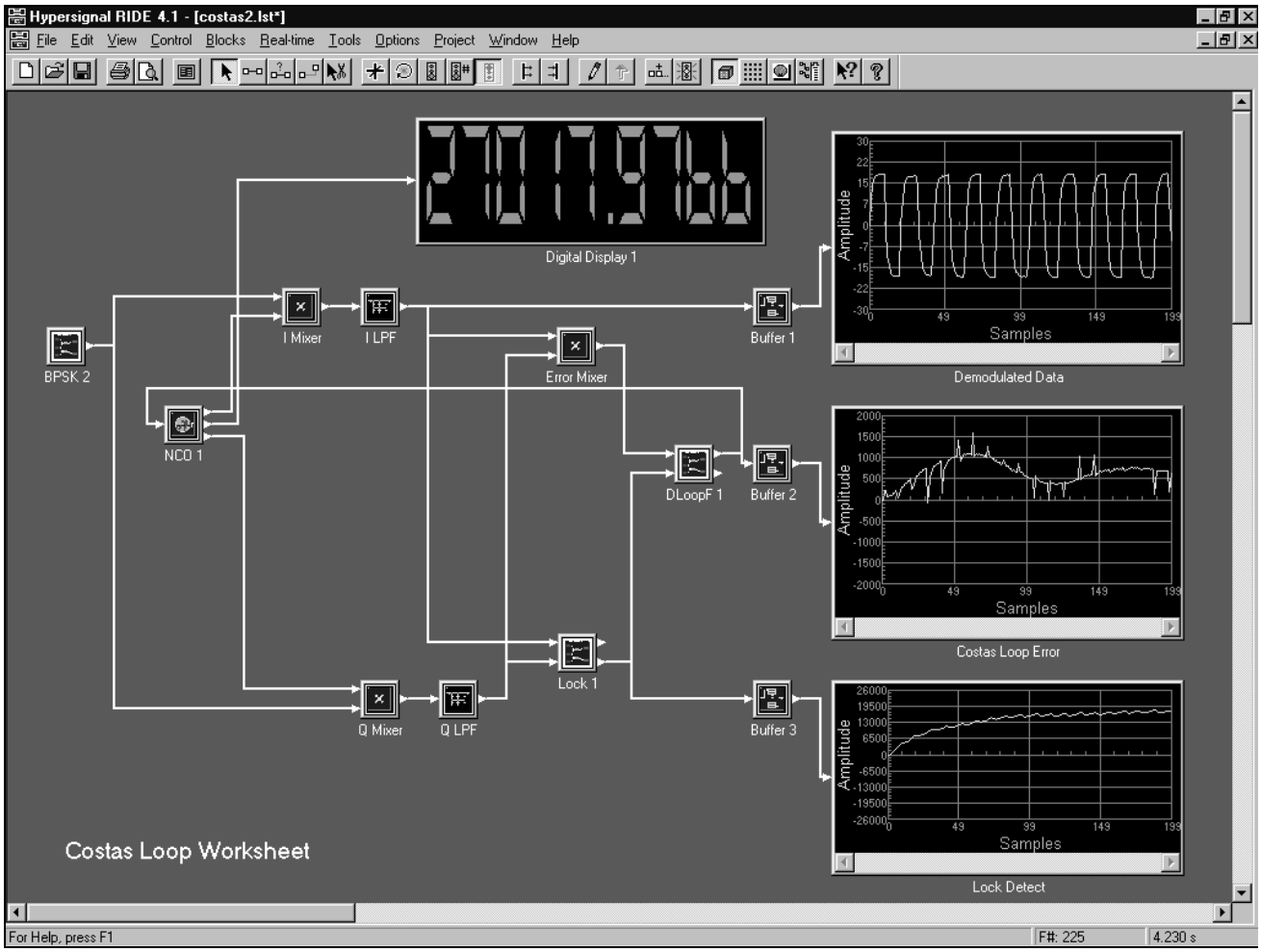

Figure 6. Costas Loop Block Diagram Worksheet

In the worksheet, the carrier input signal is a BPSK signal generated by a hierarchy BPSK block which is shown in Figure 7, the NCO block performs the VCO function, and two multiply blocks are used as in-phase mixer and quadrature mixer to perform the phase detector function. The I LPF block performs an in-phase low pass filter. The Q LPF block performs the quadrature low pass filter. The Error mixer is performed by another multiply block. The hierarchy DLOOPF block shown in Figure 8 performs the dynamic loop filtering (the bandwidth narrows when the transition from acquisition to tracking mode is made) of the first order. The Recursion block performs the feedback and initially forces the NCO block input data ready. The power and lock detects are performed by the hierarchy Lock block shown in Figure 9. The worksheet is processed sample by sample, so the Buffer blocks are needed to temporarily store samples for later display. The top display shows the demodulated data, the middle display shows the Costas loop error, and the bottom display shows the lock detector output. A Text Display is used to show the instantaneous frequency of NCO.

Note that Costas loop error is in a transient state during carrier acquisition and then stabilizes when the loop is phase-locked. The effect of the phase-locking is illustrated by the data demodulated from the I arm.

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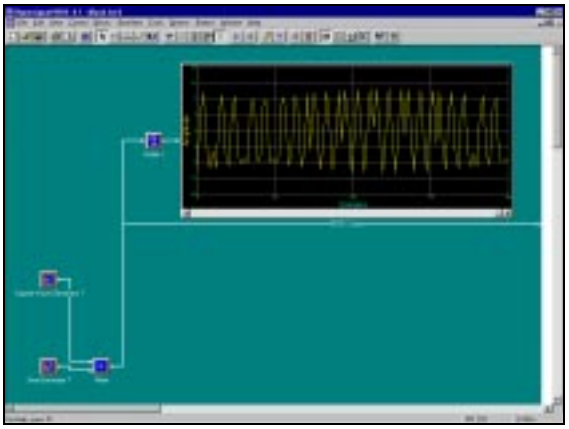

Figure 7. BPSK Hierarchy Block

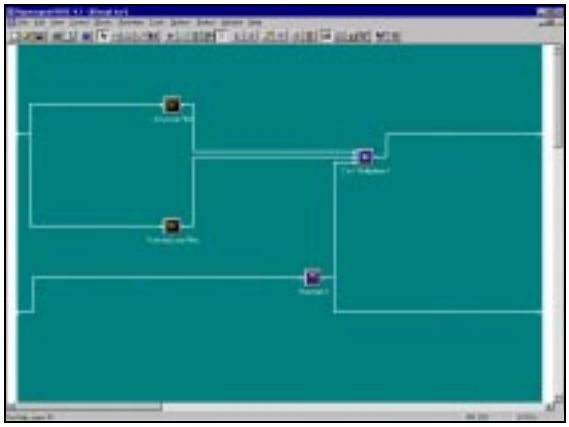

Figure 8. Dynamic Loop Filter

Figure 7 shows the structure of the hierarchy BPSK block, which consists of a Square wave generator, a Sine wave generator, a Mixer block to perform multiplication of two input waveforms, and a Buffer block used to store data samples for display. While the data display shows the BPSK carrier. As shown in Figure 8, the hierarchy block for dynamic loop filter includes an Acquisition Loop Filter, Tracking Loop Filter, Threshold, and 2 to 1 Multiplexer blocks. It has two input connections and two output connections. The top input connection is from Error Mixer block, and the bottom input connection is from Lock Detect block (bottom output connection). The top output connection is for the filtered Costas loop error, and bottom output connection is for loop filter status checking. When the lock detect value is less than the threshold value, the Acquisition Loop Filter is used, and status is 0, otherwise, the Tracking Loop Filter is used, and the status is 1.

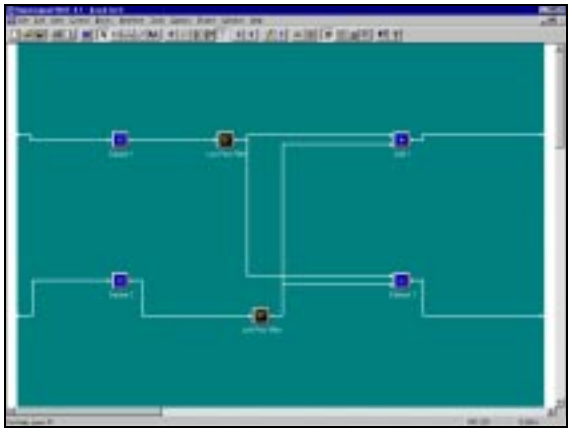

Figure 9. Lock Hierarchy Block

Figure 9 shows the structure of the hierarchy Lock block consisting of Square blocks, Low Pass Filters blocks, Add and Subtract blocks. It has two input connections and two output connections. The top input connection is from the in-phase low pass filter, and the bottom input connection is from the quadrature low pass filter. The top output connection is used for power detect, and the bottom output connection is used for lock detect.

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Code Generation

Our final step here generates an ANSI C code representation of the Block Diagram worksheet. Figure 10 shows the code generator output screen and Figure 11 shows the project view of the Costas Loop hierarchy. The code produced is easily cross-compiled for use on the target architecture.

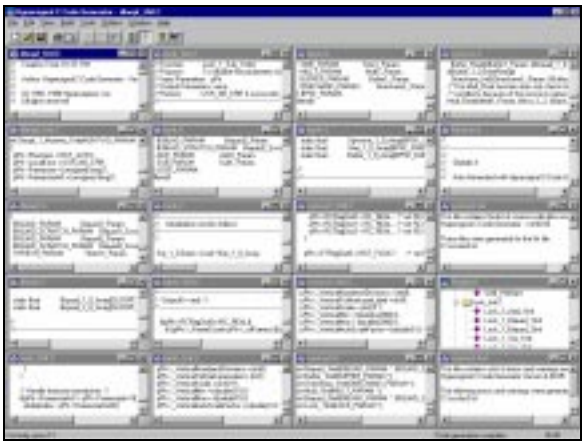

Figure 10. ANSI C code generation

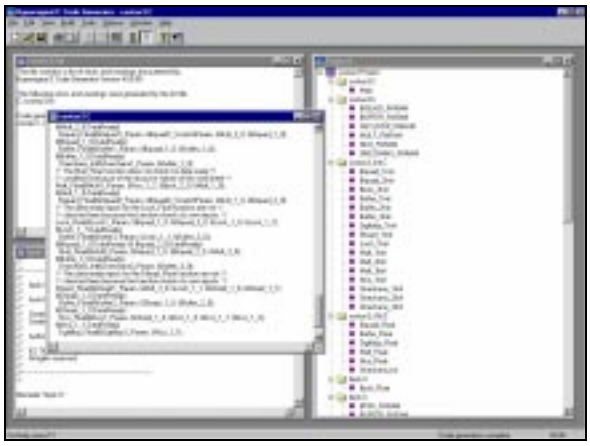

Figure 11. Project view within Hypersignal CCG

Conclusion

The Costas Loop design presented above is only one example of the powerful and flexible capabilities of Hypersignal Block Diagram/RIDE. The entire design has been conducted in the Block Diagram/RIDE without the need for writing time-consuming simulation code required by traditional methods. Complex functions such as the low pass arm filters, loop filter and NCO have been accurately modeled thanks to the rich Hypersignal Block Diagram/RIDE library – RIDE Standard Edition has more than 500 function blocks. The optional libraries such as the Advanced Transmission (Communications) Library, Advanced Speech Library, and the Image Processing Library are also available. Furthermore, The open architecture of the Hypersignal Block Diagram/RIDE allows virtually limitless simulation/modeling to be performed for proof of concept designs, saving valuable engineering mantime.

Applications

Carrier recovery for modulation/demodulation communications systems.

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