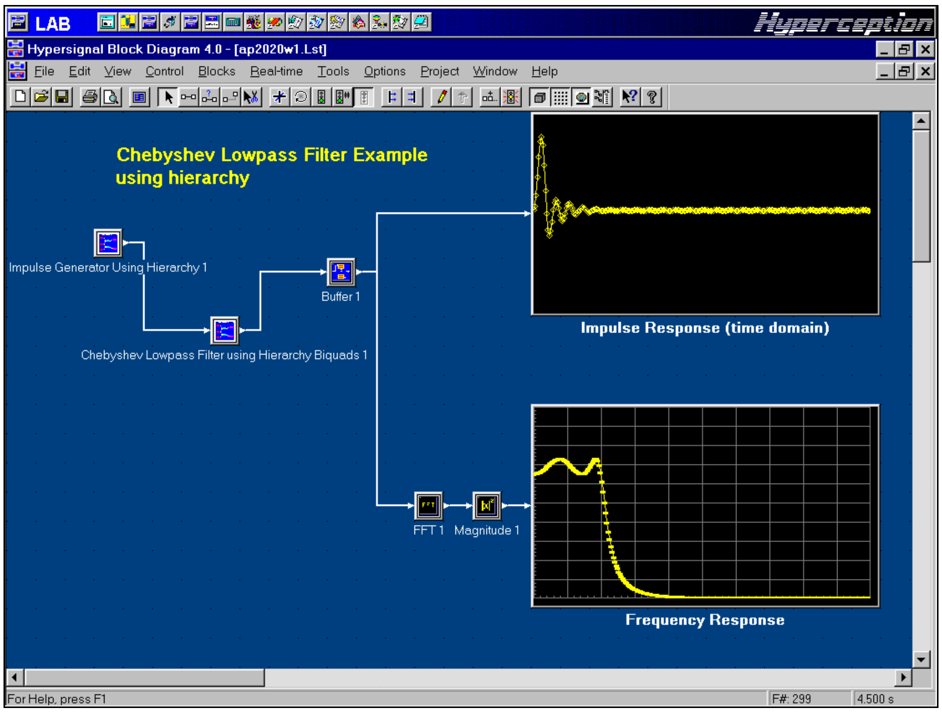
THIS APPLICATION CAN BE DONE USING:

PRODUCTS
Block Diagram
RIDE
ImPro Lab
VIDSP Studio
VIDSP Suite
OORVL Design Studio

IIR Chebyshev Lowpass Filter Design with Hypersignal® Block Diagram

Overview

A 4th-order IIR Chebyshev lowpass filter is designed using two different methods in this Hypersignal Block Diagram (or Hypersignal RIDE™, since RIDE is a superset of Block Diagram) application note. Although the Hypersignal software includes a dedicated filter design utility (which is not used in this application note), this example will demonstrate how such a filter can be constructed from low-level block functions.



Chebyshev Lowpass Filter Implementation using hierarchy

This design serves as a useful tutorial for employing recursive feedback loops, delay elements, and incorporating hierarchical design, and demonstrates the practical usability of Hypersignal Block Diagram's capability for handling recursive algorithms. Additionally, this application will utilize another important feature of Hypersignal Block Diagram, namely hierarchy.

Product Specific Information

This application could be designed using any edition of Hypersignal Block Diagram or Hypersignal RIDE (Standard Edition, Professional Edition, or Enterprise Edition). In this example, no DSP/Acquisition board is needed, as the PC is doing all the processing; however, it would be relatively easy to implement this in real-time using a DSP/Acquisition board in conjunction with Hypersignal RIDE.

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Detailed Description

Chebyshev filters have the property that the magnitude of the frequency response is either equiripple in the passband and monotonic in the stopband or monotonic in the passband and equiripple in the stopband. The former case is that of Chebyshev I type filters and the latter case is that of Chebyshev II type filters. This design example allows for the distribution of error uniformly across the entire passband.

The digital filter for this 4th-order Chebyshev I digital lowpass filter is expressed as follows:

$$H(z) = \frac{0.001836(1+z^{-1})^4}{(1-1.4996z^{-1}+0.84z^{-2})(1-1.5548z^{-1}+0.6493z^{-2})}$$

This transfer function will be implemented in Hypersignal Block Diagram/RIDE as seen in the following discussion.

Implementation

This IIR filter application will be accomplished using two different methods.

The first method involves constructing the filter through use of low-level block functions to implement the 4th-order Chebyshev I lowpass filter described by the transfer function above. This design is an excellent tutorial for employing hierarchical design, delay elements, and recursive feedback loops in a design.

The second method is a much faster implementation, which replaces the hierarchical biquad worksheets with high-level biquad block functions. This implementation does not require use of a buffer block because processing is done frame-by-frame instead of point-by-point.

The following block functions and hierarchy blocks are used in this example:

Block Function	Description
PULSE (hierarchy)	impulse generator
CHEB (hierarchy)	lowpass filter
BIQUAD (hierarchy)	biquad section – used in CHEB
BIQUAD (hierarchy)	biquad section [second instance]
Buffer	data buffer accumulation
Gain	Used in BIQUAD - gain stage
Delay	Used in BIQUAD - Sample Delay
5-input Add	Used in BIQUAD - sum
FFT	map to frequency domain
Magnitude	linear magnitude
Constant Generator	Used in PULSE to create impulse
Subtract	Used in PULSE to create impulse
Single-Channel Display	Graphical display

Table of block functions used in method one

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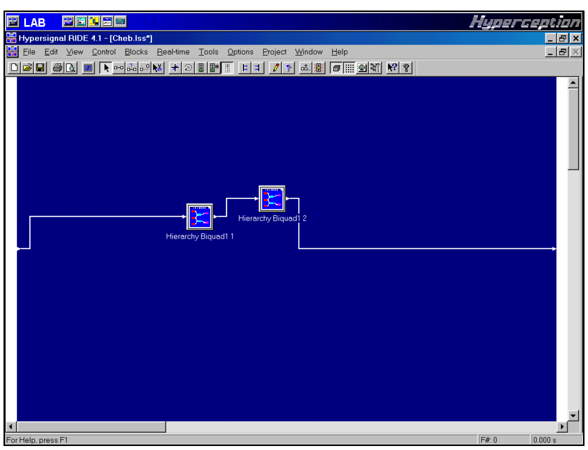
Method One

The actual lowpass filter in this method is found in the CHEB hierarchy block, which is constructed from two hierarchical biquad sections. To compute the frequency response of the filter, the filter is first hit with an impulse. The impulse signal is generated by the PULSE hierarchy block.

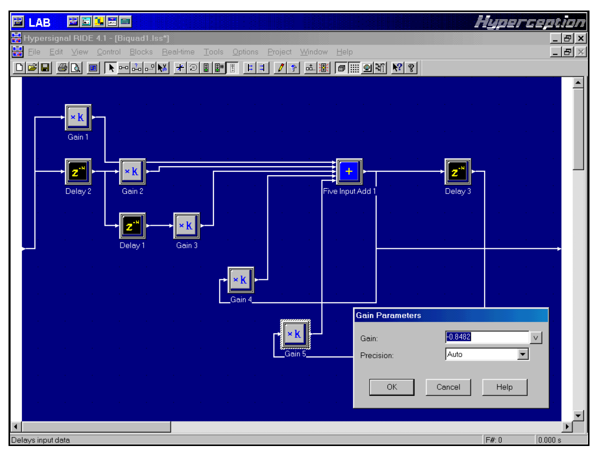
It is important to note that the framesize used for this example has been set to one. That is, the filter will produce one data sample output for every Block Diagram frame processed. A buffer block is used to hold data values until a sufficient number of samples have been processed. When enough samples have been accumulated in the buffer block, the entire buffer of data is passed to the Fast Fourier Transform (FFT) block, for frame-based, or block processing. Blocks connected after the buffer block will not process data until the buffer block releases its data, indicating a full buffer of data. This will result in converting from single point-based processing to frame-based processing after a sufficient number of points have been accumulated.

For this example worksheet, the buffer block size is set to 25 samples, and the FFT size is set to 256 points (8th order). This means that the FFT will zero-fill the remaining 231 points in the frame prior to computing the FFT. The buffer size is set to 25 to allow for a faster execution of the worksheet, but this is user-selectable. The above display was obtained by changing the buffer block size to 256, and running the simulation.

When the buffer block releases its impulse response data, a FFT is performed on the impulse response and magnitude calculation is then computed. Both the digital frequency response and impulse response of the IIR filter are then graphically displayed. The phase response could have been easily added to the simulation.



CHEB worksheet using hierarchical biquads



BIQUAD worksheet (used twice in CHEB worksheet)

The lowpass filter implementation is computed by the CHEB hierarchy block worksheet. This worksheet can be expanded into its individual components by double clicking on the CHEB block. The resulting CHEB worksheet is shown in the figure above.

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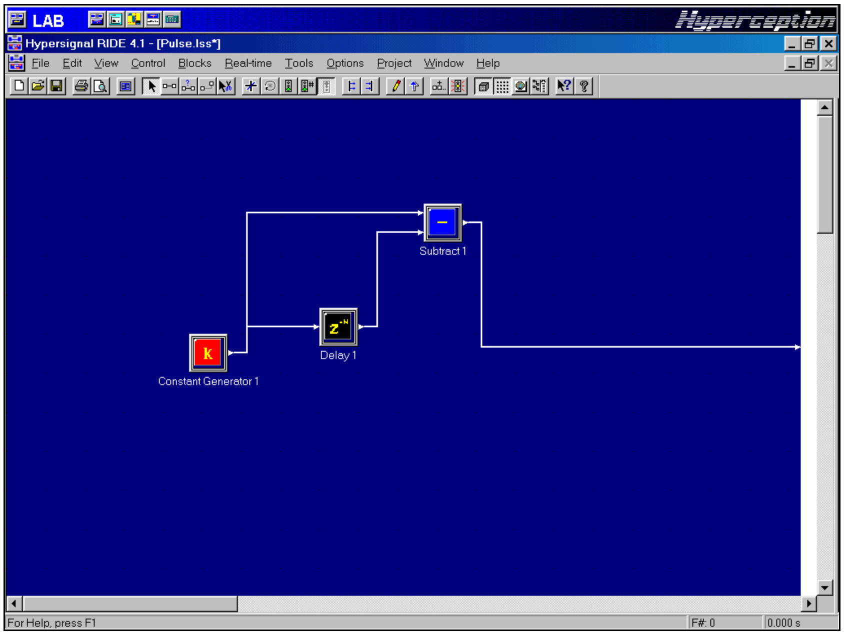
It can be seen that the CHEB worksheet is actually made-up of two hierarchy biquad blocks and a gain block. These blocks implement the transfer function of the filter, with each biquad block representing a second order section of the denominator. The biquad implementation is shown above, next to the CHEB worksheet figure.



Impulse Generator Hierarchy Worksheet (PULSE)

The Constant Generator block, whose output is delayed by one sample point and subtracted from itself, provides the impulse to the filter; this could have been easier accomplished with the Impulse Generator function as shown in the next example, but the general usefulness of this impulse generation technique was provided for the reader to generalize to other applications.

Method Two

As shown in the figure below, the second method makes use of two high-level biquad blocks to implement the low-pass filter and the results are the same as those obtained in the first method. The second implementation of the filter is faster due to its frame-based processing nature. Instead of building the biquad sections from low-level blocks such as gains, and delays with inter-block recursion, this worksheet makes use of a dedicated biquad block function. In this example, an impulse generator block function is used instead of the PULSE hierarchy block function used in the first example.

Due to the very fast speed of simulation in Hypersignal Block Diagram/RIDE, the **RUN FRAME** command is used to run only a single frame of data, since the impulse generator only produces a single impulse the first

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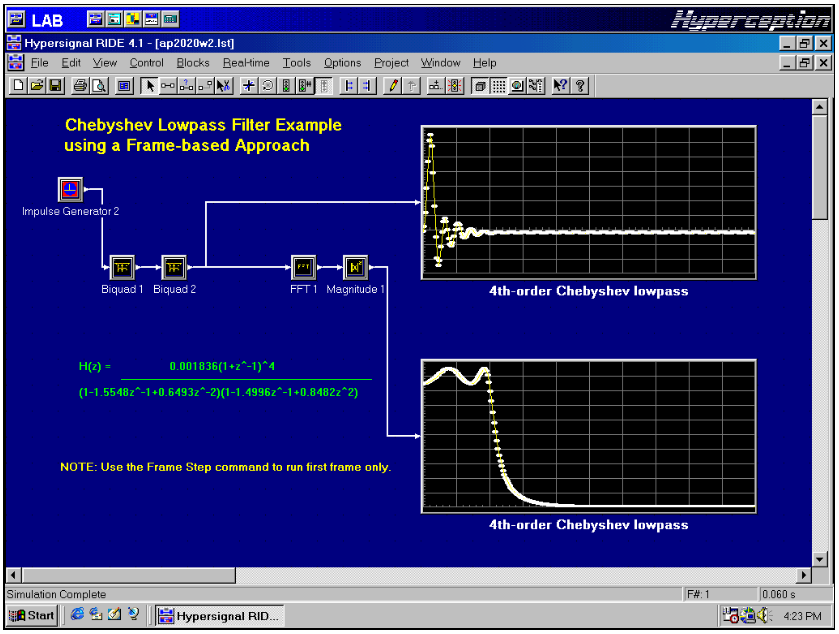
frame; all frames thereafter will produce zero output, and if the user runs the simulation continuously, the first frame will go by too fast for the user to observe!



Frame-based example Chebyshev Lowpass Filter

It is important to note that Hypersignal Block Diagram/RIDE includes a FIR/IIR filter design utility, and dedicated FIR and IIR filter blocks to provide direct filtering of signals; this application note describes lower-level methods to accomplish filtering, which is sometimes useful for research and academic applications.

Applications

The recursive feedback loops and hierarchical implementation of the lowpass digital filter in this design example can be applied to other systems, which require feedback. This includes control systems, and systems, which require delay lines. Additionally, the hierarchical design methodology employed is useful in many applications requiring sub-system design approach.

References

Alan V. Oppenheim and Ronald W. Schafer, *Digital Signal Processing*, Prentice-Hall Inc., Englewood Cliffs, NJ, 1975.

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