Creating Custom Hardware with LabVIEW

NI LabVIEW FPGA Module

- Graphically develop custom FPGA logic and download to NI reconfigurable I/O (RIO) hardware targets
- Create custom mix of analog I/O, digital I/O, counters, and triggers using off-the-shelf hardware
- Implement custom timing, triggering, and I/O logic with 25 ns resolution
- Define custom control and signal processing algorithms with loop rates up to 40 MHz
- Execute multiple tasks simultaneously with hardware determinism
- Integrate VHDL into your LabVIEW FPGA application
- Implement PC communication without developing complex driver software

FPGA Hardware Targets

- R Series DAQ devices
- CompactRIO reconfigurable embedded chassis
- Compact Vision System
- PXI timing and synchronization devices

System Requirements

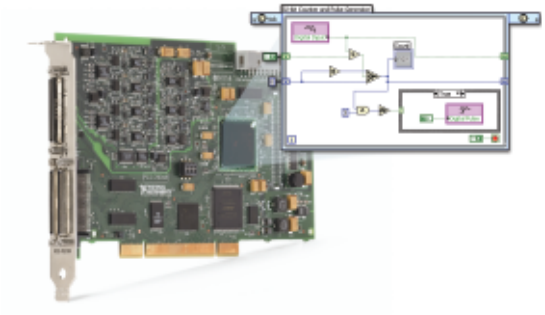
- Windows 2000/XP
- 512 MB RAM for 1M gate devices, 2 GB RAM for 3M gate devices
- 2 GB disk space

Required Software

- LabVIEW Full or Professional Development System, current version

Recommended Software

- LabVIEW Real-Time Module
- NI LabVIEW Digital Filter Design Toolkit
- NI SoftMotion Development Module for LabVIEW



Overview

The National Instruments LabVIEW FPGA Module extends LabVIEW graphical development to field-programmable gate arrays (FPGAs) on RIO hardware. Using the NI LabVIEW FPGA Module, you can develop VIs to define custom I/O and control hardware without prior knowledge of digital design or complex EDA tools. In addition, you can use the LabVIEW FPGA Module and RIO hardware to rapidly prototype and develop FPGA code. LabVIEW graphical programming is an intuitive way to program embedded devices because the block diagram of a LabVIEW FPGA VI can represent the parallelism and timing of embedded systems much better than text-based languages. After developing the FPGA VI, you can easily integrate RIO hardware with a LabVIEW (Windows) system or a LabVIEW Real-Time system.

LabVIEW FPGA and RIO technology are ideal for applications requiring custom signals. These include applications such as:

- Integrating custom timing, triggering, and synchronization
- Integrating a custom mix of analog I/O, digital I/O, counters, and triggers into a single device
- Integrating custom digital communication protocols
- Parallel processing and data acquisition
- Custom motion control
- Off-loading signal processing and control from a host PC or real-time system

The LabVIEW FPGA Module targets a growing family of NI RIO devices, as shown above. Use NI R Series data acquisition (DAQ) devices for complex DAQ or real-time I/O applications. Use the NI CompactRIO platform for modular FPGA-timed I/O with built-in signal conditioning and direct signal connectivity for maximum flexibility in embedded measurement and control applications. Develop custom FPGA logic on an NI compact vision system to add custom triggering, PWM signals, motion control, or custom communications protocols to machine vision applications. Implement custom timing, triggering, and synchronization routines using NI PXI timing and synchronization modules.

Graphical Development Environment

When targeted to the FPGA device, LabVIEW displays a focused palette containing only the functions that you can implement on the FPGA. Use a combination of these functions to define logic and embed intelligence in your RIO device.

The LabVIEW FPGA functions palette includes typical LabVIEW structures and functions, such as While Loops, For Loops, Case Structures, and Sequence Structures. It also includes a dedicated set of LabVIEW FPGA-specific functions for math, signal generation and analysis, linear and nonlinear control, comparison logic, array and cluster manipulation, analog and digital I/O, and timing.

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Figure 1 shows an example of a custom counter and period measurement application developed in LabVIEW and downloaded to a RIO device. The upper loop increments a 16-bit counter for every falling edge from DI 0 (digital line 0 configured for input), makes the count value available for the host application, and generates a digital pulse on DO 1 (digital line 1 configured for output) every four falling edges. The lower loop implements a period measurement by measuring the number of clock cycles between rising edges detected on a digital input line. The resolution of the measurement is determined by the loop rate.

The Single-Cycle Timed Loop structure that encloses the custom counter and period measurement code is a special implementation of the LabVIEW Timed Loop and iterates every FPGA clock cycle. In Figure 1, the block diagram includes a false Boolean constant so the loop runs continuously. The clock rate of the counter is determined by the FPGA clock rate at compile time; the default is 40 MHz. For this application, both loops execute simultaneously at 40 MHz. The code generated by the Single-Cycle Timed Loop is also more space-efficient, using fewer gates on the FPGA than LabVIEW code defined with a traditional While Loop.

Finally, you can integrate existing VHDL IP cores, such as communication protocols or filter cores, into a LabVIEW FPGA block diagram using the HDL Interface Node.

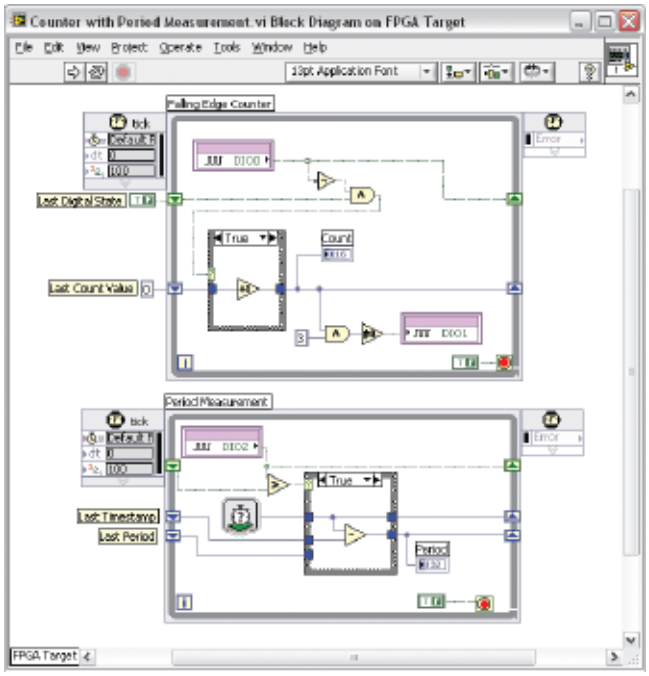


Figure 1. LabVIEW FPGA Block Diagram of a Custom Counter and Period Measurement Application

Software Structures in Hardware

Each Single-Cycle Timed Loop in Figure 1 controls the placement of registers in the FPGA. The terminals on the left and right sides of each Single-Cycle Timed Loop represent registered data on the FPGA and pass the data value from one loop iteration to the next. Each control and indicator on the front panel of the embedded VI, in this case the indicators labeled "Count" and "Period," are also implemented as registers in the FPGA; however, these registers are used to pass data to a host application. Finally, the DI and DO terminals read data directly from the FPGA I/O block.

Parallel Execution

LabVIEW graphical programming is the ideal way to represent the parallelism of FPGA hardware. Compiled LabVIEW FPGA code is implemented in hardware by configuring logic cell resources on the FPGA. Independent sections of code, such as parallel loops, are implemented as independent sections of the FPGA. After the chip is configured, data is clocked through the device at a rate specified by the onboard clock, executing independent areas of the chip simultaneously. Figure 1 illustrates how the parallelism of LabVIEW FPGA enables the loops to execute simultaneously without competing for execution resources.

System Architectures

With the LabVIEW FPGA Module, you develop LabVIEW FPGA programs on a Windows development system. Then LabVIEW compiles the code for FPGA synthesis on the NI RIO device. Once downloaded to the target, the embedded LabVIEW FPGA VI can execute in one of the following three different configurations:

- Autonomously, where the FPGA device runs independently of other systems
- Combined with a PC running LabVIEW for Windows, where data transfers from the FPGA device to the PC for off-line floating-point analysis, networking, file I/O, or graphical user interface display
- Combined with a LabVIEW Real-Time system, where data is transferred from the FPGA device to a dedicated processor running a real-time OS

The LabVIEW Real-Time system provides a deterministic processing engine for functions performed synchronously or asynchronously to the FPGA. For example, floating-point arithmetic, including FFTs, PID calculations, and custom control algorithms, are often performed in the LabVIEW Real-Time environment. You can store relevant data on a LabVIEW Real-Time system or transfer it to a LabVIEW for Windows host machine for off-line analysis, data logging, or user interface displays. This configuration is shown in Figure 2.

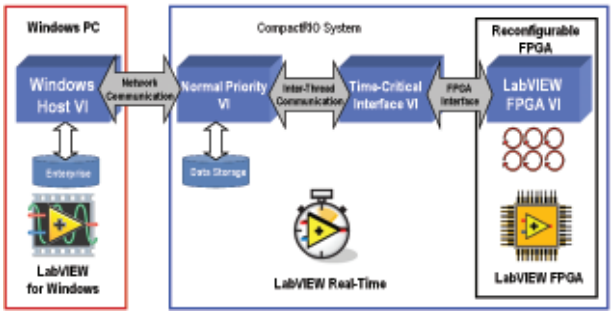
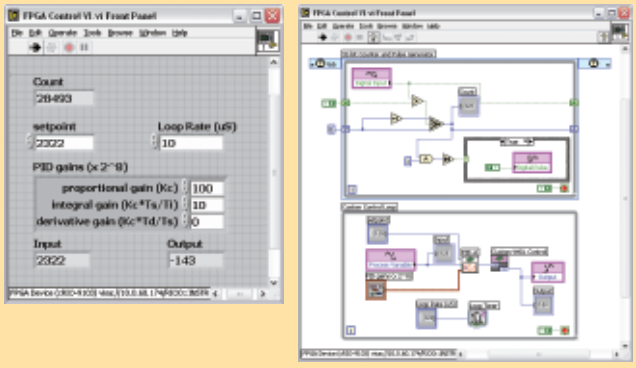


Figure 2. LabVIEW FPGA Architecture with LabVIEW Real-Time and Windows Host PC

From a LabVIEW Real-Time or LabVIEW for Windows application, you can easily access data in the FPGA registers, represented as controls and indicators on the LabVIEW FPGA VI, using the FPGA host interface. With the FPGA interface, a LabVIEW Real-Time or Windows application can acknowledge and clear interrupts generated in RIO hardware for single-point data or stream data from the FPGA device using DMA. Figure 3 shows a basic FPGA VI and its corresponding host VI.

LabVIEW FPGA VI



LabVIEW Host VI

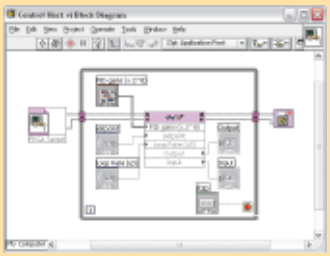


Figure 3. Embedded LabVIEW FPGA VI with Corresponding Host VI

Debugging Tools

Depending on the complexity of your code and the specifications of your development system, compile time for an FPGA VI can range from minutes to several hours. To maximize development productivity, the LabVIEW FPGA Module includes a bit-accurate emulation mode for R Series devices so you can verify the logic of your design before initiating the compile process. While targeted to the FPGA emulator, LabVIEW accesses I/O from the device and executes the VI logic on the Windows machine. In this mode, you can use the same debugging tools available in LabVIEW for Windows, such as execution highlighting, probes, and breakpoints.

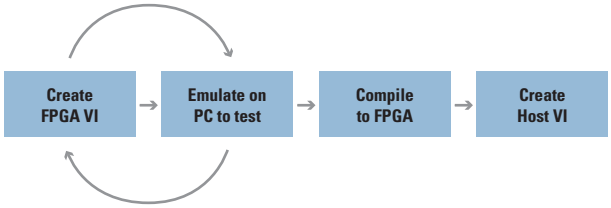


Figure 4. LabVIEW FPGA Application Development Flow

LabVIEW FPGA Hardware Targets

R Series Intelligent DAQ Devices

NI PCI or PXI R Series intelligent DAQ devices provide analog and digital data acquisition and control for high-performance, user-configurable timing and synchronization, as well as onboard decision making. With R Series reconfigurable I/O devices and LabVIEW FPGA, you can extend your PXI or PCI measurement and control system by adding user-defined hardware for operations such as custom discrete and analog control, sensor simulation, digital protocol emulation, and precise custom timing and control. These devices are available with analog and digital I/O.

Figure 5. R Series Intelligent DAQ Devices

CompactRIO

NI CompactRIO is a small, industrially rugged, modular control and acquisition platform that provides high-performance I/O and unprecedented flexibility in system timing. You can use CompactRIO as signal conditioning for an R Series DAQ device or build an embedded system with the CompactRIO embedded controller for applications such as machine control, in-vehicle DAQ, or mobile NVH testers. Among other industrial certifications and ratings, the CompactRIO system is designed for shock greater than 50 g and has a -40 to 70 °C temperature range.

Figure 6. CompactRIO Embedded System

Compact Vision System

The NI CVS-145x devices are rugged machine vision packages that withstand the harsh environments common in robotics, automated test, and industrial inspection systems. CVS-145x systems offer unprecedented I/O capabilities and network connectivity for distributed machine vision applications. CVS-145x systems use IEEE 1394 (FireWire) technology, compatible with more than 40 cameras with a wide range of functionality, performance, and price. The CVS-1455 and CVS-1456 contain a configurable FPGA for implementing custom counters, timing, or motor control in your machine vision application.

Figure 7. Compact Vision System

PXI Timing and Synchronization Modules

The NI PXI-6653 and PXI-6652 timing and synchronization control modules use the trigger bus, star trigger, and system reference clock features of PXI to implement multidevice or multichassis synchronization. The LabVIEW FPGA Module targets the FPGA on the PXI-6653/2 modules to develop custom, user-defined applications that were previously impossible to implement with off-the-shelf hardware. These applications include timing and synchronization techniques, custom triggering, and high-speed analog counters.

Figure 8. PXI Timing and Synchronization Modules

Ordering Information

NI LabVIEW FPGA Module 778694-03

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2005-5696-821-101-D